HA2556/883

Wideband Four Quadrant Analog Multiplier (Voltage Output)

July 1994

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **High Speed Voltage Output. . . . . 450V/μs (Typ)**
- **Low Multiplication error . . . . . 1.5% (Typ)**
- **Input Bias Currents . . . . . 8μA (Typ)**
- **Signal Input Feedthrough . . . . . -50dB (Typ)**
- **Wide Y Channel Bandwidth . . . . . 57MHz (Typ)**
- **Wide X Channel Bandwidth . . . . . 52MHz (Typ)**
- **0.1dB Gain Flatness (V_Y) . . . . . 5.0MHz (Typ)**

Applications

- **Military Avionics**
- **Missile Guidance Systems**
- **Medical Imaging Displays**
- **Video Mixers**
- **Sonar AGC Processors**
- **Radar Signal Conditioning**
- **Voltage Controlled Amplifier**
- **Vector Generator**

Description

The HA-2556/883 is a monolithic, high speed, four quadrant, analog multiplier constructed in Intersil' Dielectrically Isolated High Frequency Process. The voltage output simplifies many designs by eliminating the current-to-voltage conversion stage required for current output multipliers. The HA-2556/883 provides a 450V/μs output slew rate and maintains 52MHz and 57MHz bandwidths for the X and Y channels respectively, making it an ideal part for use in video systems.

The suitability for precision video applications is demonstrated further by the Y Channel 0.1dB gain flatness to 5.0MHz, 1.5% multiplication error, -50dB feedthrough and differential inputs with 8μA bias current. The HA-2556 also has low differential gain (0.1%) and phase (0.1^o) errors.

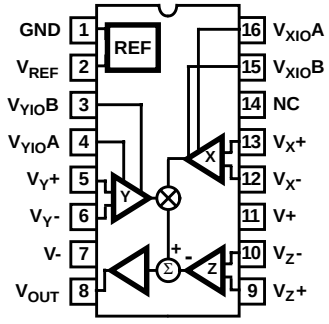
The HA-2556/883 is well suited for AGC circuits as well as mixer applications for sonar, radar, and medical imaging equipment. The HA-2556/883 is not limited to multiplication applications only; frequency doubling, power detection, as well as many other configurations are possible.

Ordering Information

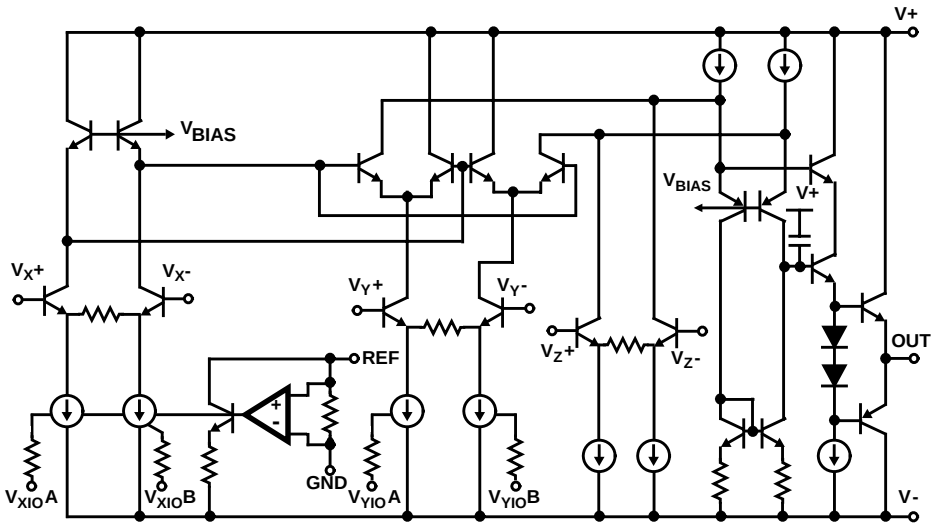
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA1-2556/883	-55^{o}C to +125^{o}C	16 Lead CerDIP

Pinout

HA-2556/883
(CERDIP)
TOP VIEW



Simplified Schematic



Spec Number **511063-883**
File Number **3619**

Absolute Maximum Ratings

Voltage Between V+ and V- 35V
Differential Input Voltage 6V
Output Current . . . . . ±40mA
ESD Rating . . . . . < 2000V
Lead Temperature (Soldering 10s) . . . . . +300°C
Storage Temperature Range . . . . . -65°C ≤ T_A ≤ +150°C
Max Junction Temperature . . . . . +175°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
CerDIP Package	82°C/W	27°C/W

Maximum Package Power Dissipation at +75°C
CerDIP Package 1.22W
Package Power Dissipation Derating Factor above +75°C
CerDIP Package . . . . . 12mW/°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Supply Voltage (±V_S) . . . . . ±15V
Operating Temperature Range . . . . . -55°C ≤ T_A ≤ +125°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: V_{SUPPLY} = ±15V, R_F = 50Ω, R_L = 1kΩ, C_L = 20pF, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Multiplication Error	ME	V_Y, V_X = ±5V	1	+25°C	-3	3	%FS
			2, 3	+125°C, -55°C	-6	6	%FS
Linearity Error	LE4V	V_Y, V_X = ±4V	1	+25°C	-0.5	0.5	%FS
	LE5V	V_Y, V_X = ±5V	1	+25°C	-1	1	%FS
Input Offset Voltage (V_X)	V_{XIO}	V_Y = ±5V	1	+25°C	-15	15	mV
			2, 3	+125°C, -55°C	-25	25	mV
Input Bias Current (V_X)	I_B (V_X)	V_X = 0V, V_Y = 5V	1	+25°C	-15	15	µA
			2, 3	+125°C, -55°C	-25	25	µA
Input Offset Current (V_X)	I_{IO} (V_X)	V_X = 0V, V_Y = 5V	1	+25°C	-2	2	µA
			2, 3	+125°C, -55°C	-3	3	µA
Common Mode (V_X) Rejection Ratio	CMRR (V_X)	V_XCM = ±10V, V_Y = 5V	1	+25°C	65	-	dB
			2, 3	+125°C, -55°C	65	-	dB
Power Supply (V_X) Rejection Ratio	+PSRR (V_X)	V_{CC} = +12V to +17V, V_Y = 5V	1	+25°C	65	-	dB
			2, 3	+125°C, -55°C	65	-	dB
	-PSRR (V_X)	V_{EE} = -12V to -17V, V_Y = 5V	1	+25°C	45	-	dB
			2, 3	+125°C, -55°C	45	-	dB
Input Offset Voltage (V_Y)	V_{YIO}	V_X = ±5V	1	+25°C	-15	15	mV
			2, 3	+125°C, -55°C	-25	25	mV
Input Bias Current (V_Y)	I_B (V_Y)	V_Y = 0V, V_X = 5V	1	+25°C	-15	15	µA
			2, 3	+125°C, -55°C	-25	25	µA
Input Offset Current (V_Y)	I_{IO} (V_Y)	V_Y = 0V, V_X = 5V	1	+25°C	-2	2	µA
			2, 3	+125°C, -55°C	-3	3	µA
Common Mode (V_Y) Rejection Ratio	CMRR (V_Y)	V_YCM = +9V, -10V, V_X = 5V	1	+25°C	65	-	dB
			2, 3	+125°C, -55°C	65	-	dB
Power Supply (V_Y) Rejection Ratio	+PSRR (V_Y)	V_{CC} = +12V to +17V, V_X = 5V	1	+25°C	65	-	dB
			2, 3	+125°C, -55°C	65	-	dB
	-PSRR (V_Y)	V_{EE} = -12V to -17V, V_X = 5V	1	+25°C	45	-	dB
			2, 3	+125°C, -55°C	45	-	dB

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: V_{SUPPLY} = ±15V, R_F = 50Ω, R_L = 1kΩ, C_L = 20pF, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage (V_Z)	V_{ZIO}	V_X = 0V, V_Y = 0V	1	+25°C	-15	15	mV
			2, 3	+125°C, -55°C	-25	25	mV
Input Bias Current (V_Z)	I_B (V_Z)	V_X = 0V, V_Y = 0V	1	+25°C	-15	15	µA
			2, 3	+125°C, -55°C	-25	25	µA
Input Offset Current (V_Z)	I_{IO} (V_Z)	V_X = 0V, V_Y = 0V	1	+25°C	-2	2	µA
			2, 3	+125°C, -55°C	-3	3	µA
Common Mode (V_Z) Rejection Ratio	CMRR (V_Z)	V_ZCM = ±10V V_X = 0V, V_Y = 0V	1	+25°C	65	-	dB
			2, 3	+125°C, -55°C	65	-	dB
Power Supply (V_Z) Rejection Ratio	+PSRR (V_Z)	V_{CC} = +12V to +17V V_X = 0V, V_Y = 0V	1	+25°C	65	-	dB
			2, 3	+125°C, -55°C	65	-	dB
	-PSRR (V_Z)	V_{EE} = -12V to -17V V_X = 0V, V_Y = 0V	1	+25°C	45	-	dB
			2, 3	+125°C, -55°C	45	-	dB
Output Current	$+I_{OUT}$	V_{OUT} = 5V, R_L = 250Ω	1	+25°C	20	-	mA
			2, 3	+125°C, -55°C	20	-	mA
	$-I_{OUT}$	V_{OUT} = 5V, R_L = 250Ω	1	+25°C	-	-20	mA
			2, 3	+125°C, -55°C	-	-20	mA
Output Voltage Swing	$+V_{OUT}$	R_L = 250Ω	1	+25°C	5	-	V
			2, 3	+125°C, -55°C	5	-	V
	$-V_{OUT}$	R_L = 250Ω	1	+25°C	-	-5	V
			2, 3	+125°C, -55°C	-	-5	V
Supply Current	$\pm I_{CC}$	V_X, V_Y = 0V	1	+25°C	-	22	mA
			2, 3	+125°C, -55°C	-	22	mA

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Table 2 Intentionally Left Blank. See AC Specifications in Table 3.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested: at V_{SUPPLY} = ±15V, R_F = 50Ω, R_L = 1kΩ, C_L = 20pF, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
V_Y, V_Z CHARACTERISTICS (NOTE 2)							
Bandwidth	BW(V_Y)	-3dB, V_X = 5V, $V_Y \leq 200mV_{P-P}$	1	+25°C	30	-	MHz
Gain Flatness	GF(V_Y)	0.1dB, V_X = 5V, $V_Y \leq 200mV_{P-P}$	1	+25°C	4.0	-	MHz
AC Feedthrough	V_{ISO}	f_O = 5MHz, $V_Y = 200mV_{P-P}$ V_X = Nulled	1, 3	+25°C	-	-45	dB
Rise and Fall Time	T_R, T_F	V_Y = 200mV Step, V_X = 5V, 10% to 90% pts	1	+25°C	-	9.5	ns
			1	+125°C, -55°C	-	10	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested: at V_{SUPPLY} = ±15V, R_F = 50Ω, R_L = 1kΩ, C_L = 20pF, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Overshoot	+OS, -OS	V_Y = 200mV step, V_X = 5V	1	+25°C	-	35	%
			1	+125°C, -55°C	-	50	%
Slew Rate	+SR, -SR	V_Y = 10V step, V_X = 5V	1	+25°C	410	-	V/µs
			1	+125°C, -55°C	360	-	V/µs
Differential Input Resistance	R_{IN} (V_Y)	V_Y = ±5V, V_X = 0V	1	+25°C	650	-	kΩ
V_X CHARACTERISTICS							
Bandwidth	BW (V_X)	-3dB, V_Y = 5V, $V_X \leq 200mV_{P-P}$	1	+25°C	30	-	MHz
Gain Flatness	GF (V_X)	0.1dB, V_Y = 5V, $V_X \leq 200mV_{P-P}$	1	+25°C	2.0	-	MHz
AC Feedthrough	V_{ISO}	f_O = 5MHz, $V_X = 200mV_{P-P}$ V_Y = Nulled	1, 3	+25°C	-	-45	dB
Rise & Fall Time	T_R, T_F	V_X = 200mV step, V_Y = 5V, 10% to 90% pts	1	+25°C	-	9.5	ns
			1	+125°C, -55°C	-	10	ns
Overshoot	+OS, -OS	V_X = 200mV step, V_Y = 5V	1	+25°C	-	35	%
			1	+125°C, -55°C	-	50	%
Slew Rate	+SR, -SR	V_X = 10V step, V_Y = 5V	1	+25°C	410	-	V/µs
			1	+125°C, -55°C	360	-	V/µs
Differential Input Resistance	R_{IN} (V_X)	V_X = ±5V, V_Y = 0V	1	+25°C	650	-	kΩ
OUTPUT CHARACTERISTICS							
Output Resistance	R_{OUT}	V_Y = ±5V, V_X = 5V R_L = 1kΩ to 250Ω	1	+25°C	-	1	Ω

NOTES:

1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
2. V_Z AC characteristics may be implied from V_Y due to the use of V_Z as feedback in the test circuit.
3. Offset voltage applied to minimize feedthrough signal.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLE 1)
Interim Electrical Parameters (Pre Burn-In)	-
Final Electrical Test Parameters	1 (Note 1), 2, 3
Group A Test Requirements	1, 2, 3
Groups C and D Endpoints	1

NOTE:

1. PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

Die Characteristics

DIE DIMENSIONS:
71mils x 100mils x 19mils ± 1mils

METALLIZATION:
Type: Al, 1% Cu
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos)
Silox Thickness: 12kÅ ± 2kÅ
Nitride Thickness: 3.5kÅ ± 1.5kÅ

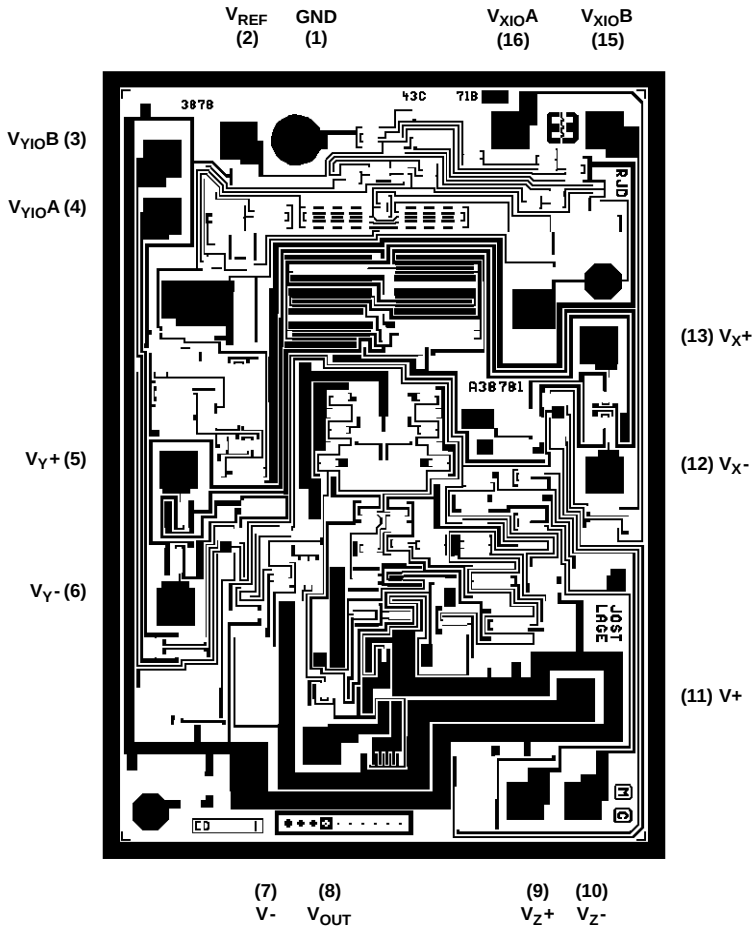
TRANSISTOR COUNT: 84

SUBSTRATE POTENTIAL: V-

WORST CASE CURRENT DENSITY:
$0.47 \times 10^5 A/cm^2$

Metallization Mask Layout

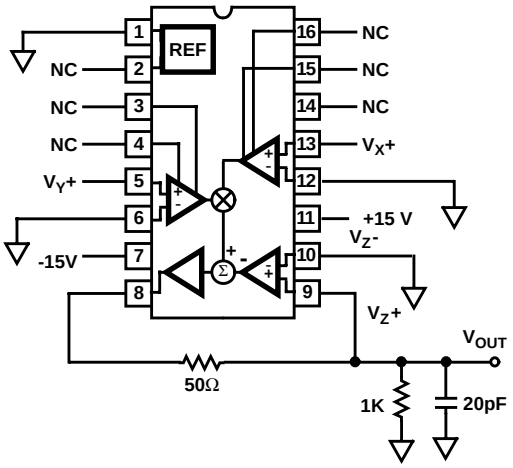
HA-2556/883



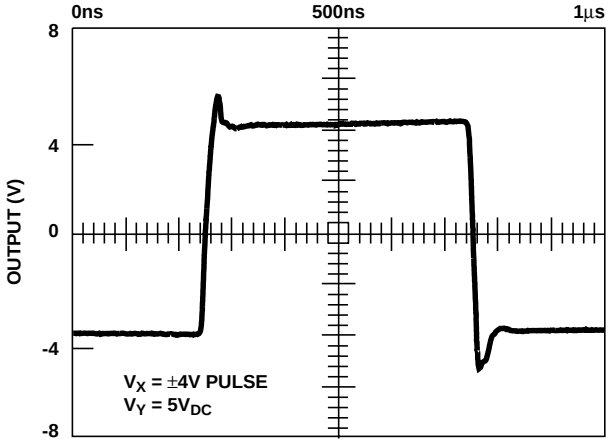
Spec Number **511063-883**

Test Waveforms

LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT

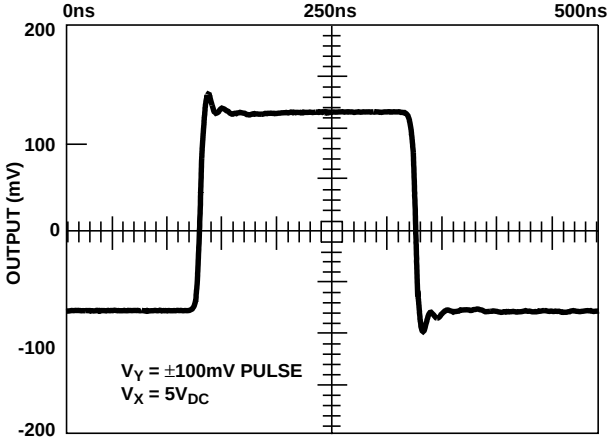


LARGE SIGNAL RESPONSE



2V/DIV; 100ns/DIV

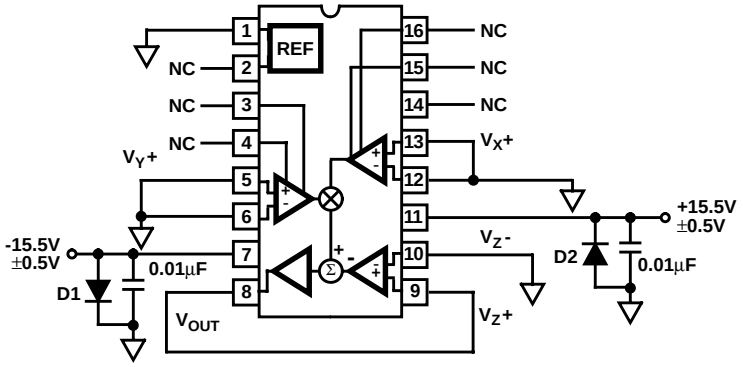
SMALL SIGNAL RESPONSE



50mV/DIV; 50ns/DIV

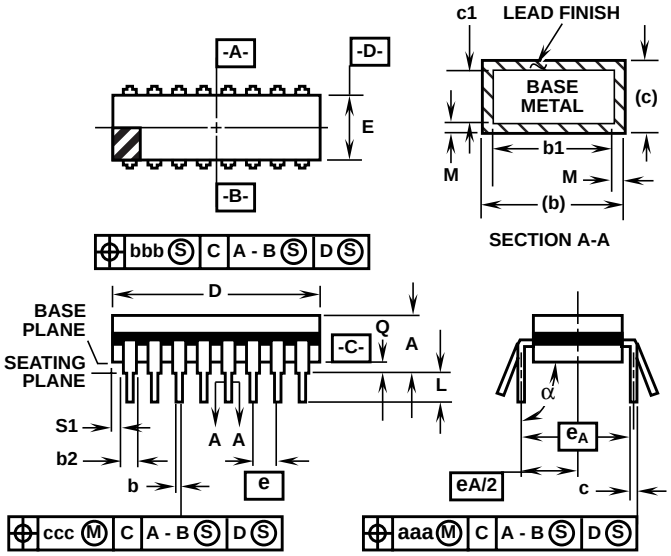
Burn-In Circuit

HA-2556/883 CERAMIC DIP



D1 = D2 = 1N4002 OR EQUIVALENT (PER BOARD)

Packaging



F16.3 **MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)**
16 LEAD DUAL-IN-LINE FRIT-SEAL CERAMIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
S2	0.005	-	0.13	-	-
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	16		16		8

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b1.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling Dimension: Inch.
11. Lead Finish: Type A.
12. Materials: Compliant to MIL-I-38535.

DESIGN INFORMATION

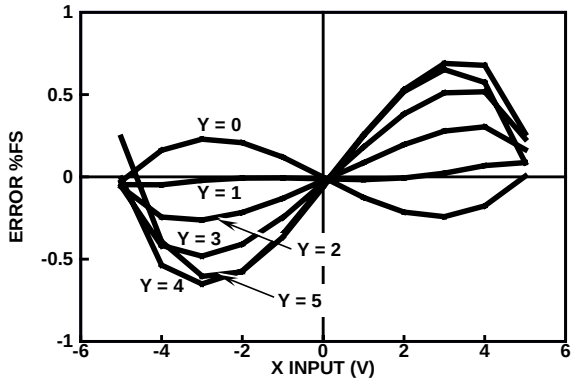
August 1999

Wideband Four Quadrant Analog Multiplier

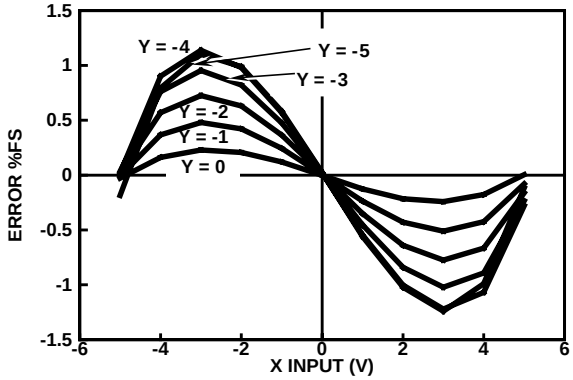
The information contained in this section has been developed through characterization by Intersil Semiconductor and is for use as application and design information only. No guarantee is implied.

Typical Performance Curves

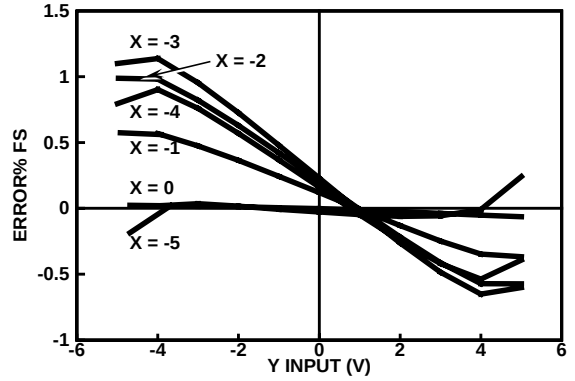
X CHANNEL MULTIPLIER ERROR



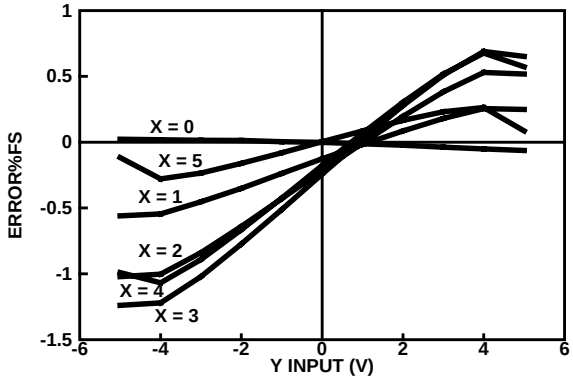
X CHANNEL MULTIPLIER ERROR



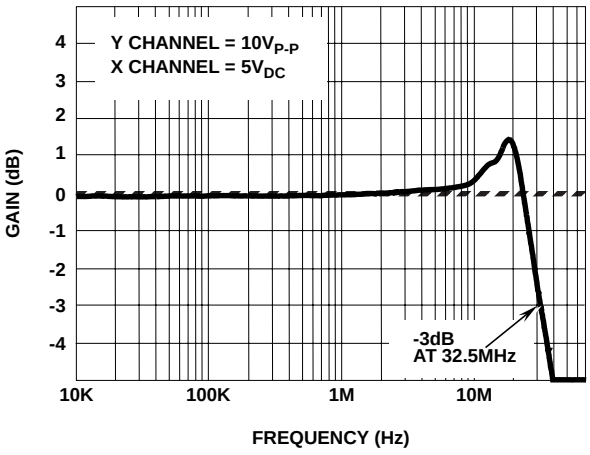
Y CHANNEL MULTIPLIER ERROR



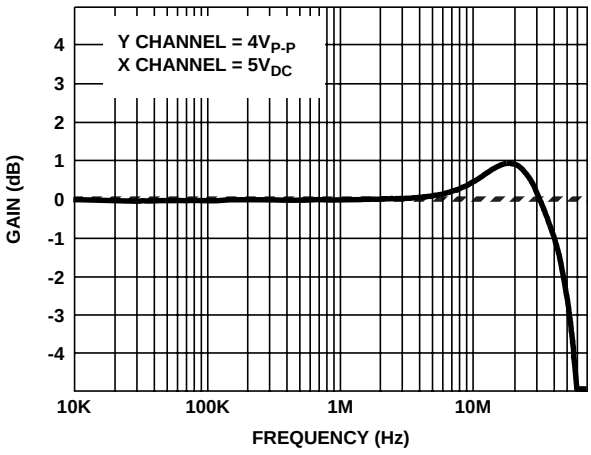
Y CHANNEL MULTIPLIER ERROR



Y CHANNEL FULL POWER BANDWIDTH



Y CHANNEL FULL POWER BANDWIDTH

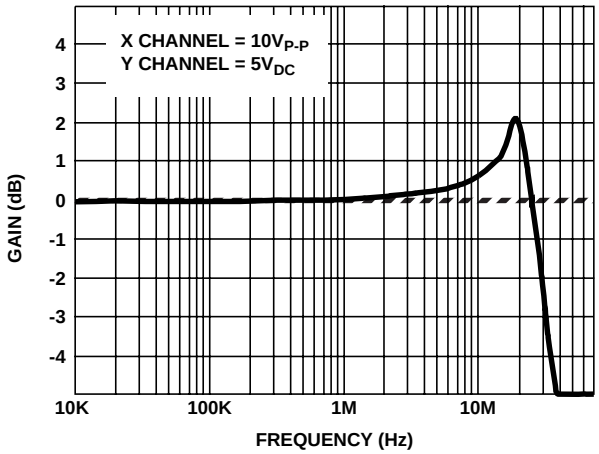


DESIGN INFORMATION (Continued)

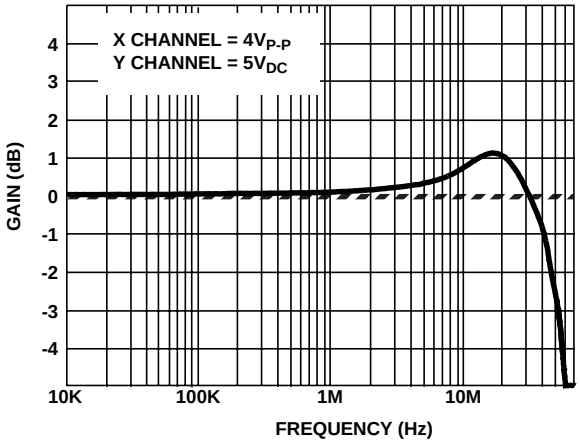
The information contained in this section has been developed through characterization by Intersil Semiconductor and is for use as application and design information only. No guarantee is implied.

Typical Performance Curves (Continued)

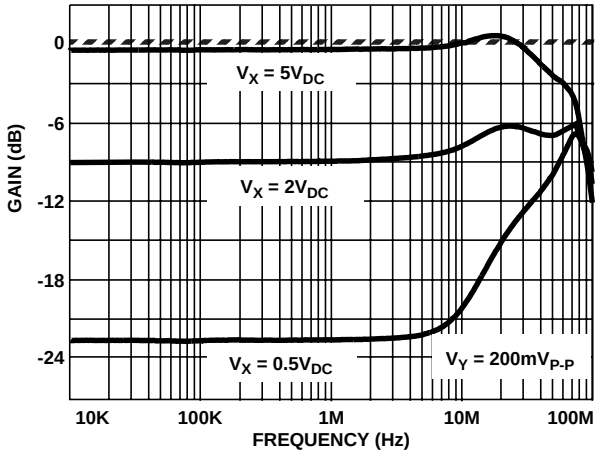
X CHANNEL FULL POWER BANDWIDTH



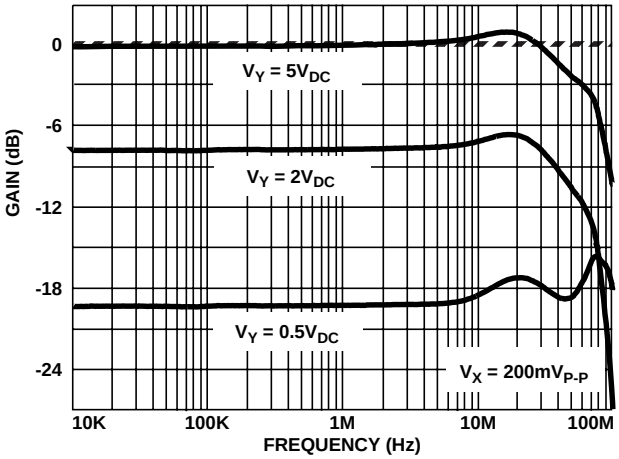
X CHANNEL FULL POWER BANDWIDTH



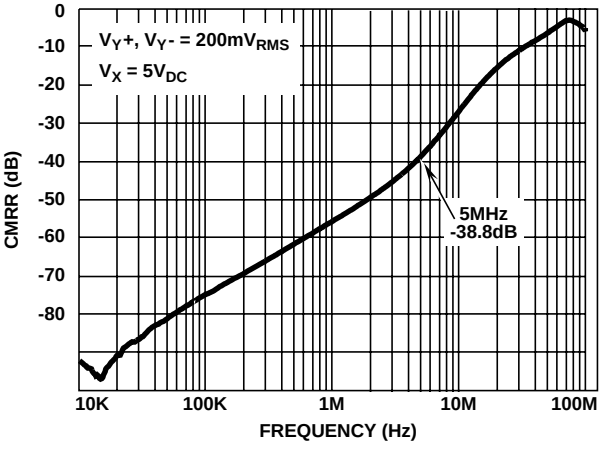
Y CHANNEL BANDWIDTH vs X CHANNEL



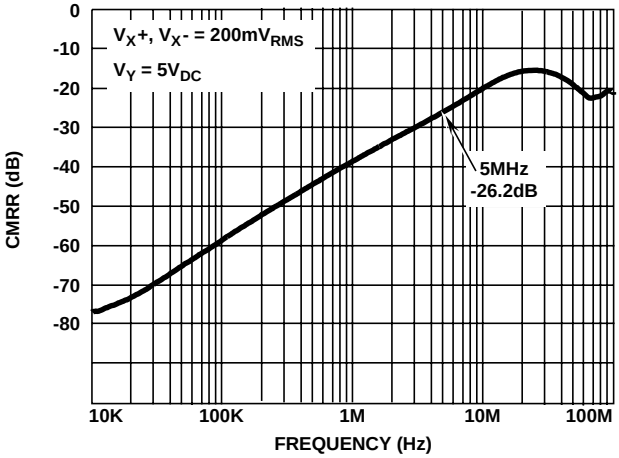
X CHANNEL BANDWIDTH vs Y CHANNEL



Y CHANNEL CMRR vs FREQUENCY



X CHANNEL CMRR vs FREQUENCY

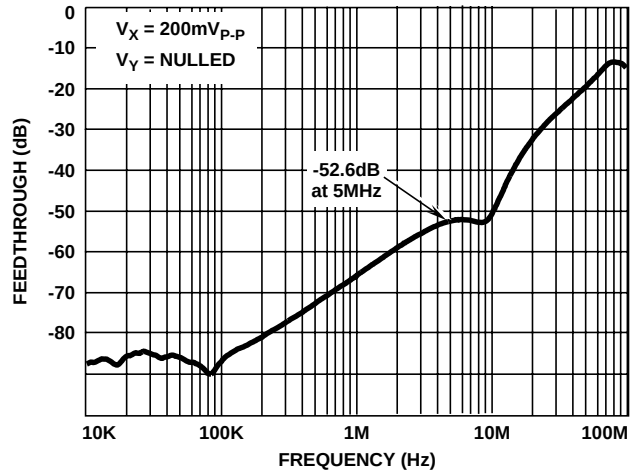


DESIGN INFORMATION (Continued)

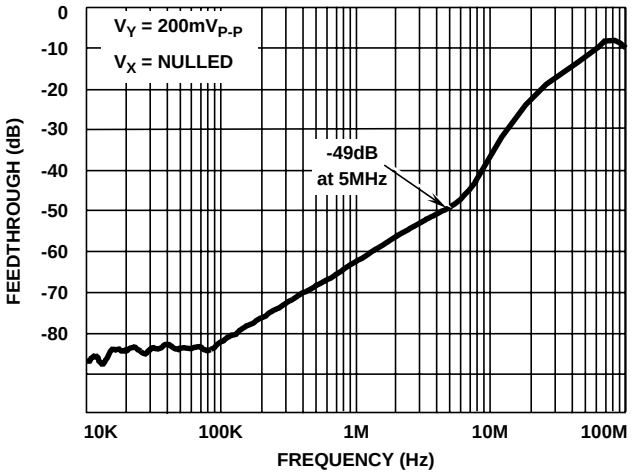
The information contained in this section has been developed through characterization by Intersil Semiconductor and is for use as application and design information only. No guarantee is implied.

Typical Performance Curves (Continued)

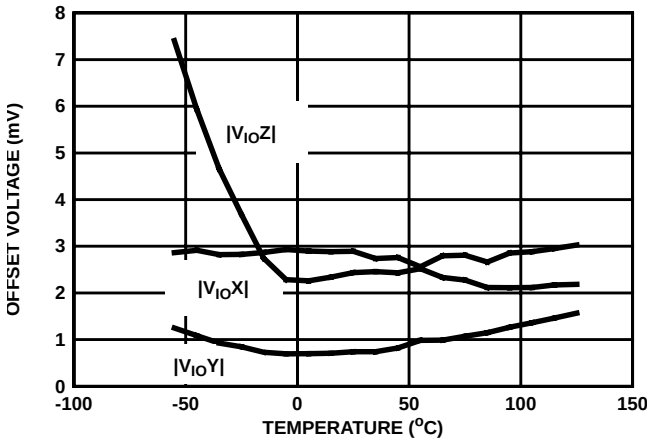
FEEDTHROUGH vs FREQUENCY



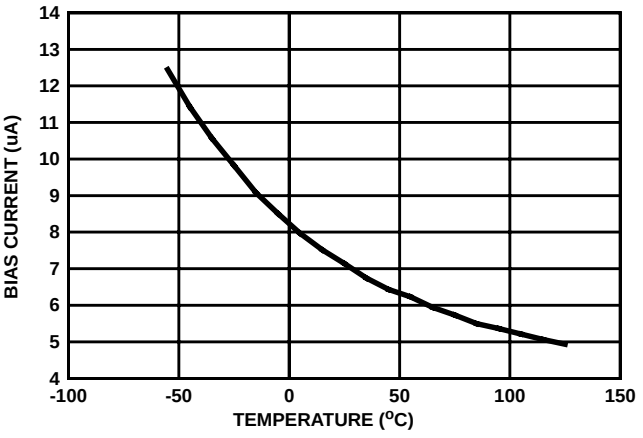
FEEDTRHOUGH vs FREQUENCY



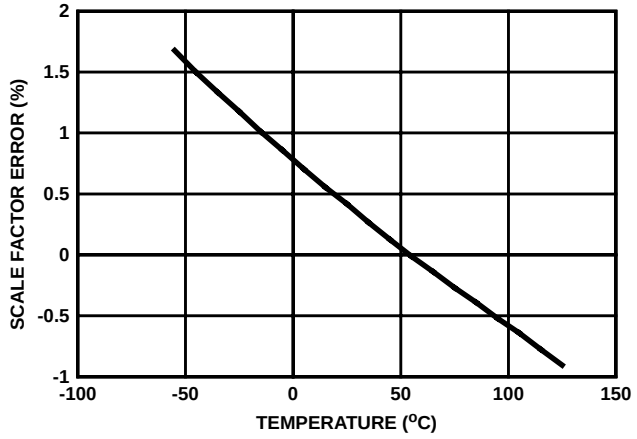
OFFSET VOLTAGE vs TEMPERATURE



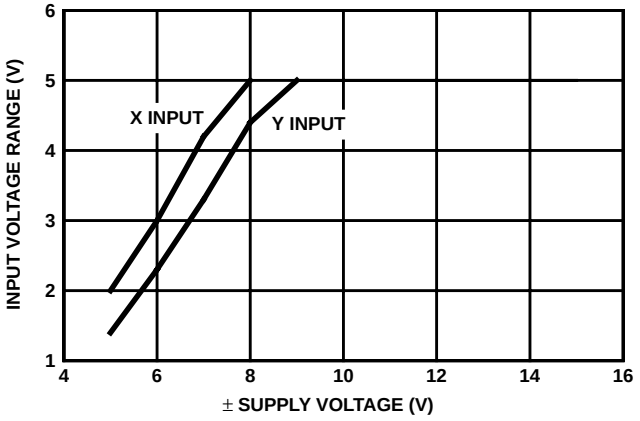
INPUT BIAS CURRENT (V_X, V_Y, V_Z) vs TEMPERATURE



SCALE FACTOR ERROR vs TEMPERATURE



INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE

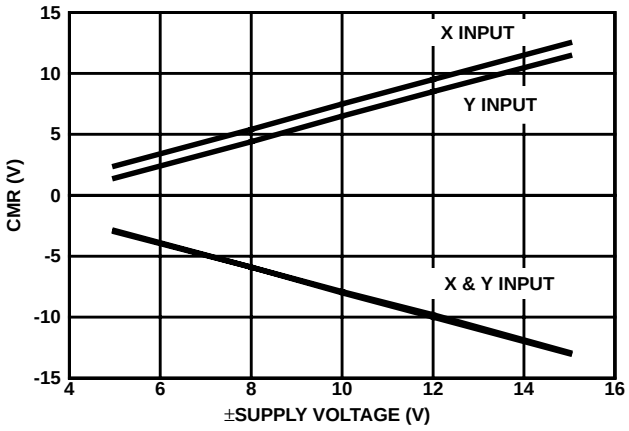


DESIGN INFORMATION (Continued)

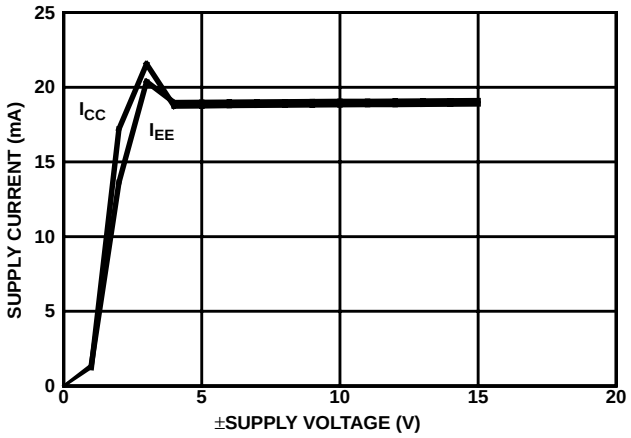
The information contained in this section has been developed through characterization by Intersil Semiconductor and is for use as application and design information only. No guarantee is implied.

Typical Performance Curves (Continued)

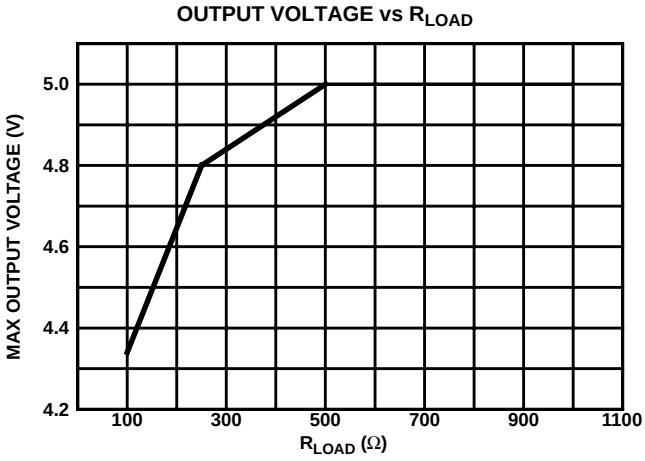
INPUT COMMON MODE RANGE vs SUPPLY VOLTAGE



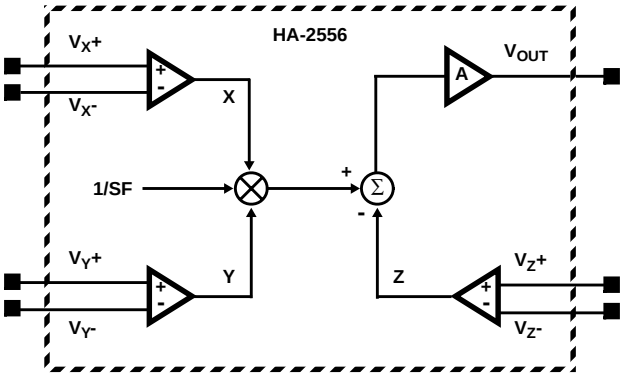
SUPPLY CURRENT vs SUPPLY VOLTAGE



OUTPUT VOLTAGE vs R_{LOAD}



Functional Block Diagram



NOTE:
The transfer equation for the HA-2556 is:
$(V_X+ - V_X-)(V_Y+ - V_Y-) = SF(V_Z+ - V_Z-)$,
where SF = Scale Factor = 5V V_X, V_Y, V_Z = Differential Inputs

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Intersil Semiconductor and is for use as application and design information only. No guarantee is implied.

Applications Information

Operation at Reduced Supply Voltages

The HA-2556 will operate over a range of supply voltages, ±5V to ±15V. Use of supply voltages below ±12V will reduce input and output voltage ranges. See “Typical Performance Curves” for more information.

Offset Adjustment

X and Y channel offset voltages may be nulled by using a 20K potentiometer between the V_{YIO} or V_{XIO} adjust pin A and B and connecting the wiper to V-. Reducing the channel offset voltage will reduce AC feedthrough and improve the multiplication error. Output offset voltage can also be nulled by connecting V_Z- to the wiper of a potentiometer which is tied between V+ and V-.

Capacitive Drive Capability

When driving capacitive loads >20pF a 50Ω resistor should be connected between V_{OUT} and V_Z+, using V_Z+ as the output (see Figure 1). This will prevent the multiplier from going unstable and reduce gain peaking at high frequencies. The 50Ω resistor will dampen the resonance formed with the capacitive load and the inductance of the output at pin 8. Gain accuracy will be maintained because the resistor is inside the feedback loop.

Theory of Operation

The HA-2556 creates an output voltage that is the product of the X and Y input voltages divided by a constant scale factor of 5V. The resulting output has the correct polarity in each of the four quadrants defined by the combinations of positive and negative X and Y inputs. The Z stage provides the means for negative feedback (in the multiplier configuration) and an input for summation into the output. This results in the following equation, where X, Y and Z are high impedance differential inputs.

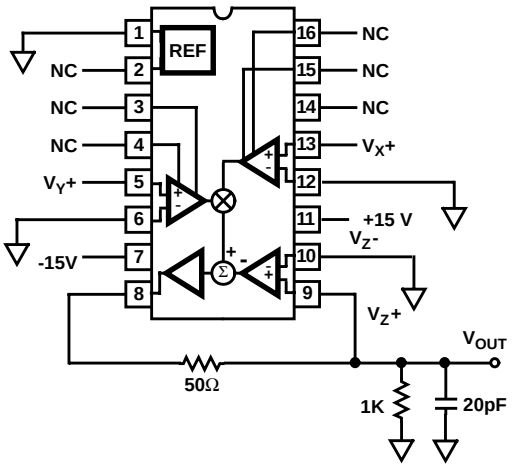


FIGURE 1. DRIVING CAPACITIVE LOAD

$$V_{OUT} = \frac{X \times Y}{5} - Z$$

To accomplish this the differential input voltages are first converted into differential currents by the X and Y input transconductance stages. The currents are then scaled by a constant reference and combined in the multiplier core. The multiplier core is a basic Gilbert Cell that produces a differential output current proportional to the product of X and Y input signal currents. This current becomes the output for the HA-2557.

The HA-2556 takes the output current of the core and feeds it to a transimpedance amplifier, that converts the current to a voltage. In the multiplier configuration, negative feedback is provided with the Z transconductance amplifier by connecting V_{OUT} to the Z input. The Z stage converts V_{OUT} to a current which is subtracted from the multiplier core before being applied to the high gain transimpedance amp. The Z stage, by virtue of it’s similarity to the X and Y stages, also cancels second order errors introduced by the dependence of V_{BE} on collector current in the X and Y stages.

The purpose of the reference circuit is to provide a stable current, used in setting the scale factor to 5V. This is achieved with a bandgap reference circuit to produce a temperature stable voltage of 1.2V which is forced across a NiCr resistor. Slight adjustments to scale factor may be possible by overriding the internal reference with the V_{REF} pin. The scale factor is used to maintain the output of the multiplier within the normal operating range of ±5V when full scale inputs are applied.

The Balance Concept

The open loop transfer equation for the HA-2556 is:

$$V_{OUT} = A\left[\frac{\left(V_{X+} - V_{X-}\right) \times \left(V_{Y+} - V_{Y-}\right)}{5} - \left(V_{Z+} - V_{Z-}\right)\right]$$

where;

A = Output Amplifier Open Loop Gain
V_X, V_Y, V_Z = Differential Input Voltages
5V = Fixed Scale Factor

An understanding of the transfer function can be gained by assuming that the open loop gain, A, of the output amplifier is infinite. With this assumption, any value of V_{OUT} can be generated with an infinitesimally small value for the terms within the brackets. Therefore we can write the equation:

$$0 = \frac{\left(V_{X+} - V_{X-}\right) \times \left(V_{Y+} - V_{Y-}\right)}{5} - \left(V_{Z+} - V_{Z-}\right)$$

which simplifies to:

$$\left(V_{X+} - V_{X-}\right) \times \left(V_{Y+} - V_{Y-}\right) = 5\left(V_{Z+} - V_{Z-}\right)$$

This form of the transfer equation provides a useful tool to analyze multiplier application circuits and will be called the Balance Concept.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Intersil Semiconductor and is for use as application and design information only. No guarantee is implied.

Let's first examine the Balance Concept as it applies to the standard multiplier configuration (Figure 2).

Signals A and B are input to the multiplier and the signal W is the result. By substituting the signal values into the Balance equation you get:

$$(A) \times (B) = 5(W)$$

And solving for W:

$$W = \frac{A \times B}{5}$$

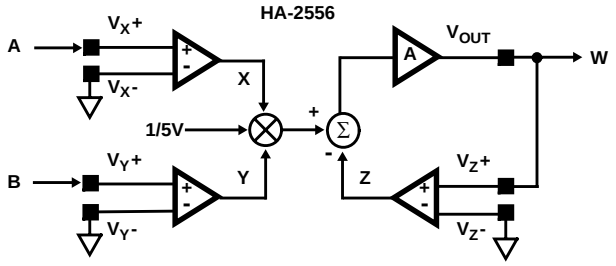


FIGURE 2. MULTIPLIER

Notice that the output (W) enters the equation in the feedback to the Z stage. The Balance Equation does not test for stability, so remember that you must provide negative feedback. In the multiplier configuration, the feedback path is connected to V_Z+ input, not V_Z-. This is due to the inversion that takes place at the summing node just prior to the output amplifier. Feedback is not restricted to the Z stage, other feedback paths are possible as in the Divider Configuration shown in Figure 3.

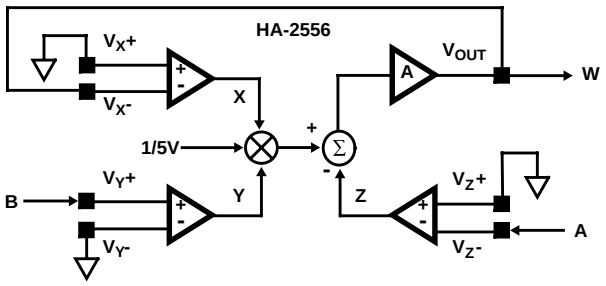


FIGURE 3. DIVIDER

Inserting the signal values A, B and W into the Balance Equation for the divider configuration yields:

$$(-W) \times (B) = 5V \times (-A)$$

Solving for W yields:

$$W = \frac{5A}{B}$$

Notice that, in the divider configuration, signal B must remain ≥0 (positive) for the feedback to be negative. If signal B is negative, then it will be multiplied by the V_X- input to produce positive feedback and the output will swing into the rail.

Signals may be applied to more than one input at a time as in the Squaring configuration in Figure 4:

Here the Balance equation will appear as:

$$(A) \times (A) = 5(W)$$

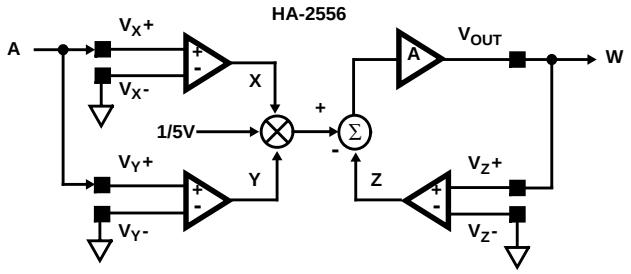


FIGURE 4. SQUARE

Which simplifies to:

$$W = \frac{A^2}{5}$$

The last basic configuration is the Square Root as shown in Figure 5. Here feedback is provided to both X and Y inputs.

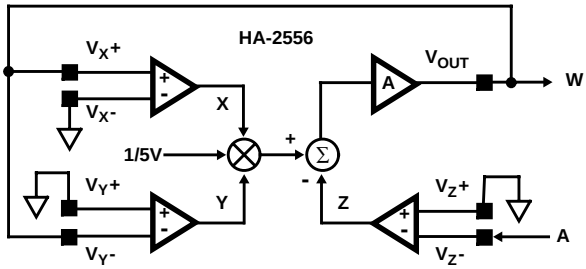


FIGURE 5. SQUARE ROOT (FOR A > 0)

The Balance equation takes the form:

$$(W) \times (-W) = 5(-A)$$

Which equates to:

$$W = \sqrt{5A}$$

Application Circuits

The four basic configurations (Multiply, Divide, Square and Square Root) as well as variations of these basic circuits have many uses.

Frequency Doubler

For example, if ACos(ωτ) is substituted for signal A in the Square function, then it becomes a Frequency Doubler and the equation takes the form:

$$(ACos(\omega\tau)) \times (ACos(\omega\tau)) = 5(W)$$

And using some trigonometric identities gives the result:

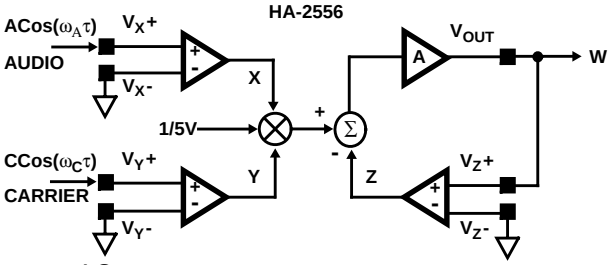
$$W = \frac{A^2}{10}(1 + Cos(2\omega\tau))$$

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Intersil Semiconductor and is for use as application and design information only. No guarantee is implied.

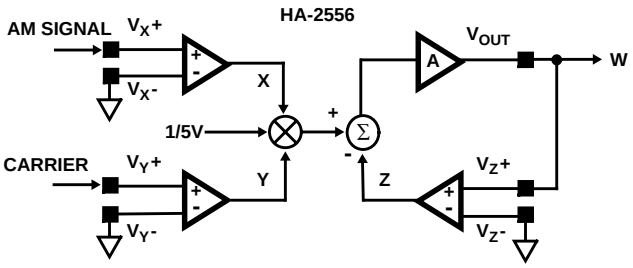
Square Root

The Square Root function can serve as a precision/wide bandwidth compander for audio or video applications. A compander improves the Signal to Noise Ratio for your system by amplifying low level signals while attenuating or compressing large signals (refer to Figure 17; $X^{0.5}$ curve). This provides for better low level signal immunity to noise during transmission. On the receiving end the original signal may be reconstructed with the standard Square function.



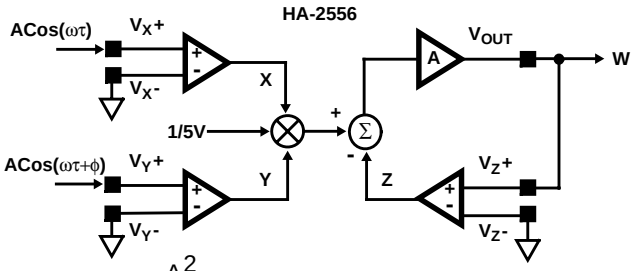
$$W = \frac{AC}{10}\left(\cos\left(\omega_C - \omega_A\right)\tau + \cos\left(\omega_C + \omega_A\right)\tau\right)$$

FIGURE 6. AM SIGNAL GENERATION



LIKE THE FREQUENCY DOUBLER YOU GET AUDIO CENTERED AT DC AND $2F_C$.

FIGURE 7. SYNCHRONOUS AM DETECTION



$$W = \frac{A^2}{10}\left(\cos\left(\phi\right) + \cos\left(2\omega\tau + \phi\right)\right)$$

DC COMPONENT IS PROPORTIONAL TO Cos(f).

FIGURE 8. PHASE DETECTION

Communications

The Multiplier configuration has applications in AM Signal Generation, Synchronous AM Detection and Phase Detection to mention a few. These circuit configurations are shown in Figure 6, Figure 7 and Figure 8. The HA-2556 is particularly useful in applications that require high speed signals on all inputs.

Each input X, Y and Z has similar wide bandwidth and input characteristics. This is unlike earlier products where one input was dedicated to a slow moving control function as is required for Automatic Gain Control. The HA-2556 is versatile enough for both.

Although the X and Y inputs have similar AC characteristics, they are not the same. The designer should consider input parameters such as small signal bandwidth, ac feedthrough and 0.1dB gain flatness to get the most performance from the HA-2556. The Y channel is the faster of the two inputs with a small signal bandwidth of typically 57MHz verses 52MHz for the X channel. Therefore in AM Signal Generation, the best performance will be obtained with the Carrier applied to the Y channel and the modulation signal (lower frequency) applied to the X channel.

Scale Factor Control

The HA-2556 is able to operate over a wide supply voltage range ±5V to ±17.5V. The ±5V range is particularly useful in video applications. At ±5V the input voltage range is reduced to ±1.4V. The output cannot reach its full scale value with this restricted input, so it may become necessary to modify the scale factor. Adjusting the scale factor may also be useful when the input signal itself is restricted to a small portion of the full scale level. Here we can make use of the high gain output amplifier by adding external gain resistors. Generating the maximum output possible for a given input signal will improve the Signal to Noise Ratio and Dynamic Range of the system. For example, let's assume that the input signals are $1V_{PEAK}$ each. Then the maximum output for the HA-2556 will be 200mV. (1V x 1V / (5V) = 200mV. It would be nice to have the output at the same full scale as our input, so let's add a gain of 5 as shown in Figure 9.

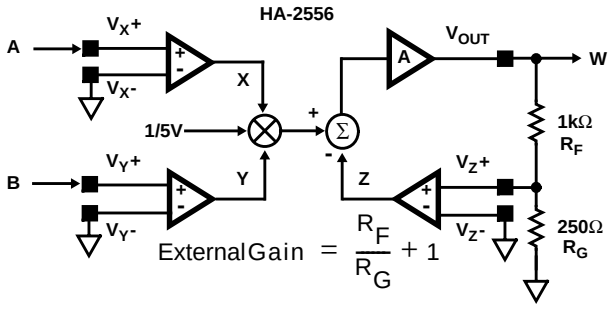


FIGURE 9. EXTERNAL GAIN OF 5

One caveat is that the output bandwidth will also drop by this factor of 5. The multiplier equation then becomes:

$$W = \frac{5AB}{5} = A \times B$$

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Intersil Semiconductor and is for use as application and design information only. No guarantee is implied.

Current Output

Another useful circuit for low voltage applications allows the user to convert the voltage output of the HA2556 to an output current. The HA-2557 is a current output version offering 100MHz of bandwidth, but its scale factor is fixed and does not have an output amplifier for additional scaling. Fortunately the circuit in Figure 10 provides an output current that can be scaled with the value of $R_{CONVERT}$ and provides an output impedance of typically 1MΩ. The equation for I_{OUT} becomes:

$$I_{OUT} = \frac{A \times B}{5} \times \frac{1}{R_{CONVERT}}$$

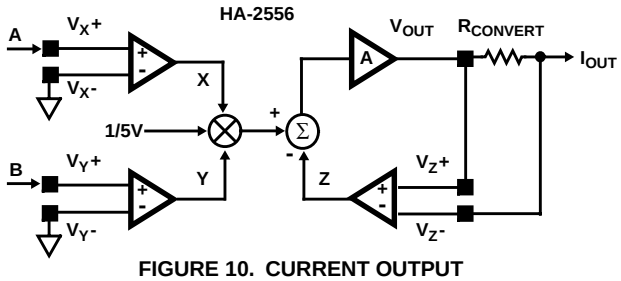


FIGURE 10. CURRENT OUTPUT

Video Fader

The Video Fader circuit provides a unique function. Here Ch B is applied to the minus Z input in addition to the minus Y input. In this way, the function in Figure 11 is generated. V_{MIX} will control the percentage of Ch A and Ch B that are mixed together to produce a resulting video image or other signal.

The Balance equation looks like:

$$(V_{MIX}) \times (ChA - ChB) = 5(V_{OUT} - ChB)$$

Which simplifies to:

$$V_{OUT} = ChB + \frac{V_{MIX}}{5}(ChA - ChB)$$

When V_{MIX} is 0V the equation becomes V_{OUT} = Ch B and Ch A is removed, conversely when VMIX is 5V the equation becomes V_{OUT} = Ch A eliminating Ch B. For VMIX values 0V ≤ VMIX ≤ 5V the output is a blend of Ch A and Ch B.

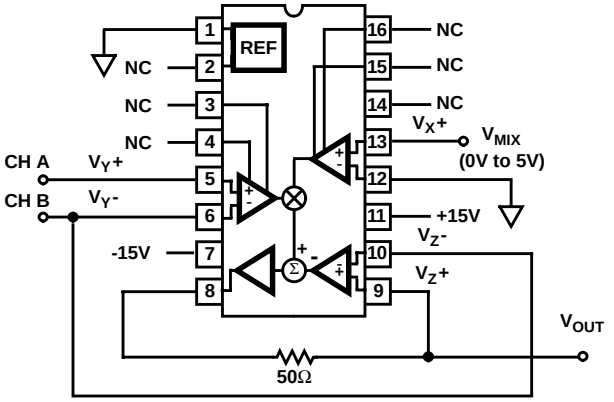


FIGURE 11. VIDEO FADER

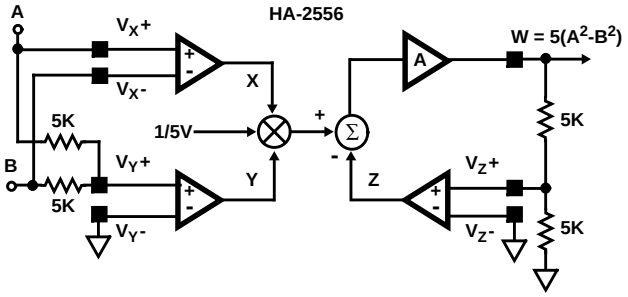
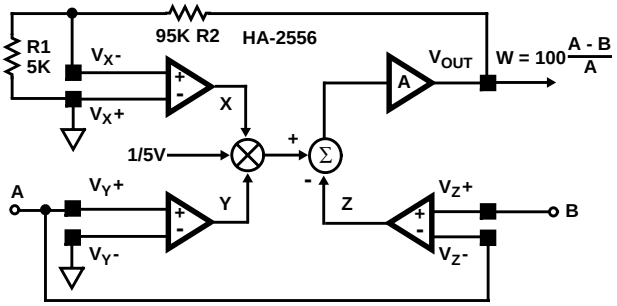


FIGURE 12. DIFFERENCE OF SQUARES



R1 and R2 set scale to 1V/%, other scale factors possible for A ≥ 0V.

FIGURE 13. PERCENTAGE DEVIATION

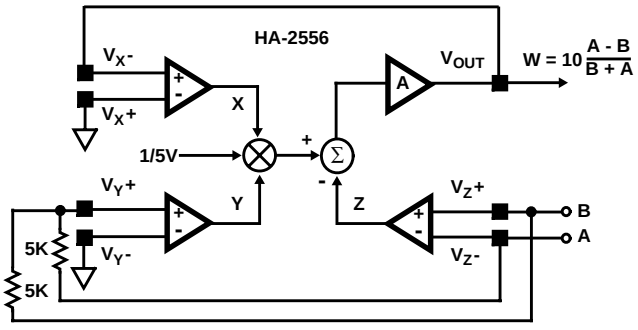


FIGURE 14. DIFFERENCE DIVIDED BY SUM (FOR A + B ≥ 0V)

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Intersil Semiconductor and is for use as application and design information only. No guarantee is implied.

Other Applications

As shown above, a function may contain several different operators at the same time and use only one HA-2556. Some other possible multi-operator functions are shown in Figure 12, Figure 13 and Figure 14.

Of course the HA-2556 is also well suited to standard multiplier applications such as Automatic Gain Control and Voltage Controlled Amplifier.

Automatic Gain Control

Figure 15 shows the HA-2556 configured in an Automatic Gain Control or AGC application. The HA-5127 low noise amplifier provides the gain control signal to the X input. This control signal sets the peak output voltage of the multiplier to match the preset reference level. The feedback network around the HA-5127 provides a response time adjustment. High frequency changes in the peak are rejected as noise or the desired signal to be transmitted. These signals do not indicate a change in the average peak value and therefore no gain adjustment is needed. Lower frequency changes in the peak value are given a gain of -1 for feedback to the control input. At DC the circuit is an integrator automatically compensating for Offset and other constant error terms.

This multiplier has the advantage over other AGC circuits, in that the signal bandwidth is not affected by the control signal gain adjustment.

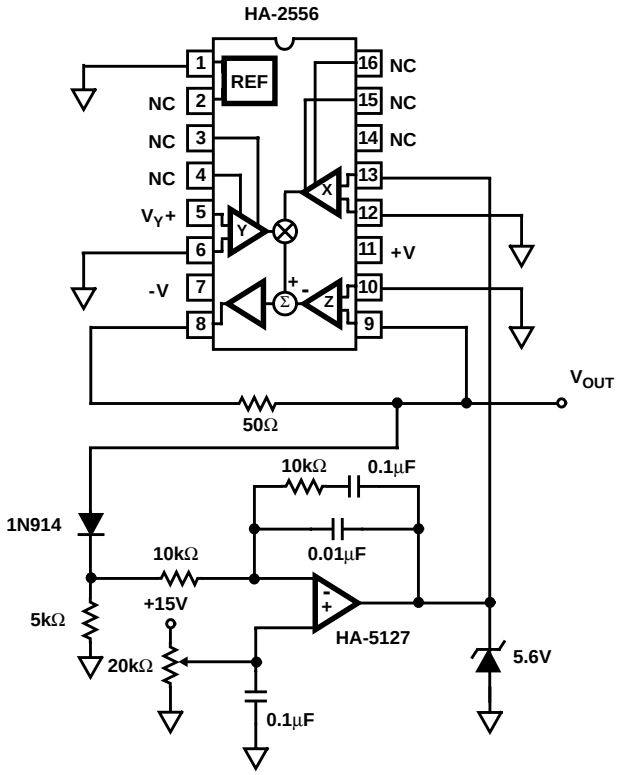


FIGURE 15. AUTOMATIC GAIN CONTROL

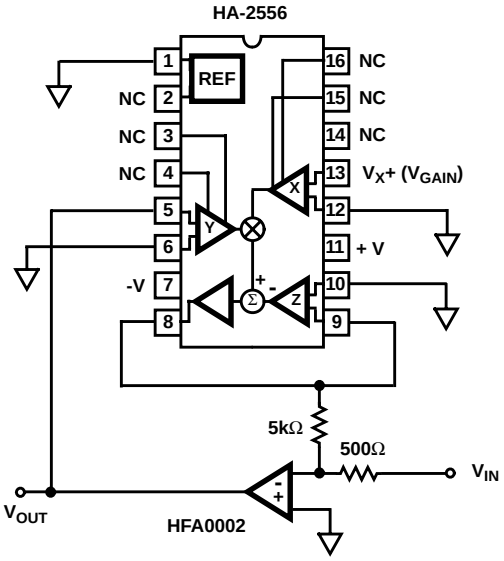


FIGURE 16. VOLTAGE CONTROLLED AMPLIFIER

Voltage Controlled Amplifier

A wide range of gain adjustment is available with the Voltage Controlled Amplifier configuration shown in Figure 16. Here the gain of the HFA0002 can be swept from 20V/V to a gain of almost 1000V/V with a DC voltage from 0 to 5V.

Wave Shaping Circuits

Wave shaping or curve fitting is another class of application for the analog multiplier. For example, where a non-linear sensor requires corrective curve fitting to improve linearity the HA-2556 can provide nonintegral powers in the range 1 to 2 or nonintegral roots in the range 0.5 to 1.0 (refer to Further Reading). This effect is displayed in Figure 17.

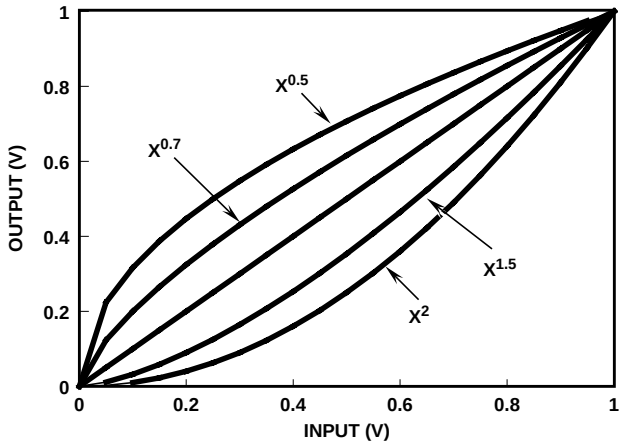


FIGURE 17. EFFECT OF NONINTEGRAL POWERS / ROOTS

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Intersil Semiconductor and is for use as application and design information only. No guarantee is implied.

Well, OK a multiplier can't do nonintegral roots "exactly" but we can get very close. We can approximate nonintegral roots with equations of the form:

$$V_o = (1-\alpha)V_{IN}^2 + \alpha V_{IN}$$

$$V_o = (1-\alpha)V_{IN}^{1/2} + \alpha V_{IN}$$

Figure 18 compares the function $V_{OUT} = V_{IN}^{0.7}$ to the approximation $V_{OUT} = 0.5V_{IN}^{0.5} + 0.5V_{IN}$.

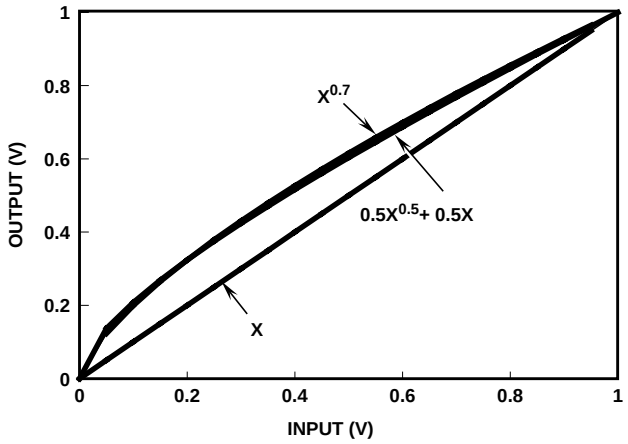


FIGURE 18. COMPARE APPROXIMATION TO NONINTEGRAL ROOT

This function can be easily built using an HA-2556 and a potentiometer for easy adjustment as shown in Figures 19 and 20. If a fixed nonintegral power is desired, the circuit shown in Figure 21 eliminates the need for the output buffer amp. These circuits approximate the function V_{IN}^M where M is the desired nonintegral power or root.

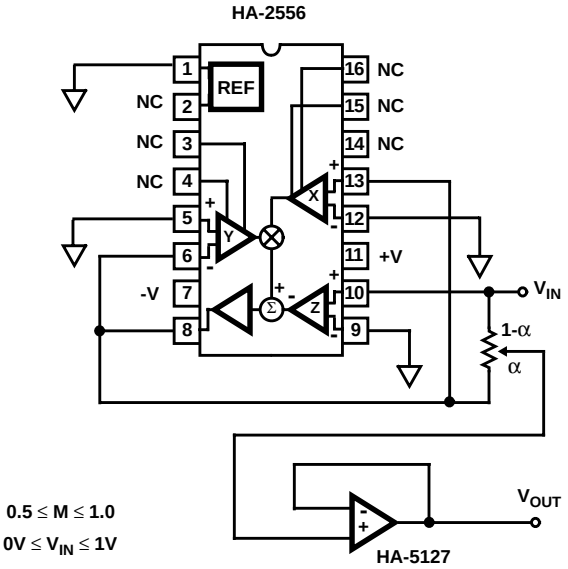


FIGURE 19. NONINTEGRAL ROOTS - ADJUSTABLE

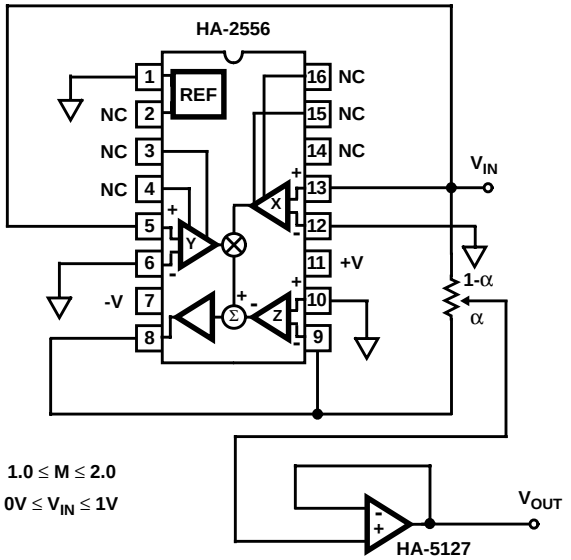
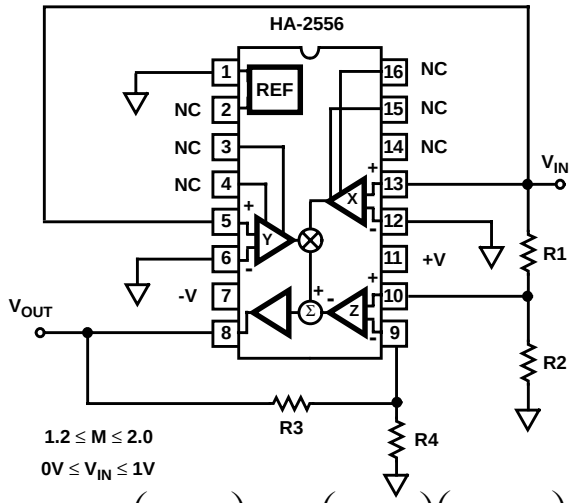


FIGURE 20. NONINTEGRAL POWERS - ADJUSTABLE



$$V_{OUT} = \frac{1}{5}\left(\frac{R3}{R4}+1\right)V_{IN}^2 + \left(\frac{R3}{R4}+1\right)\left(\frac{R2}{R1+R2}\right)V_{IN}$$

Setting:

$$1-\alpha = \frac{1}{5}\left(\frac{R3}{R4}+1\right) \qquad \alpha = \left(\frac{R3}{R4}+1\right)\left(\frac{R2}{R1+R2}\right)$$

FIGURE 21. NONINTEGRAL POWERS - FIXED

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Intersil Semiconductor and is for use as application and design information only. No guarantee is implied.

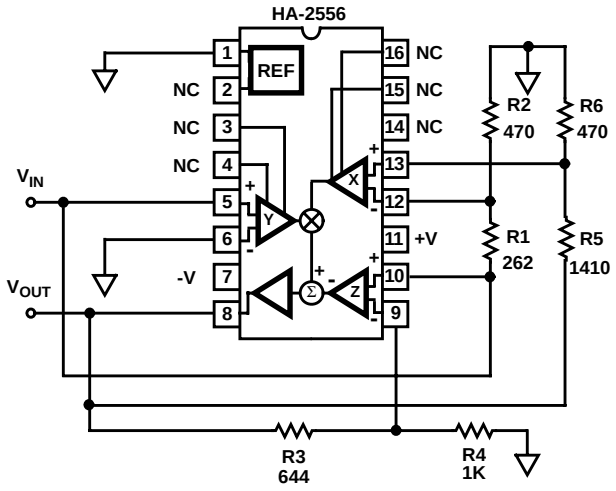
Values for α to give a desired M root or power are as follows:

ROOTS - FIGURE 19		POWERS - FIGURE 20	
M	α	M	α
0.5	0	1.0	1
0.6	≈0.25	1.2	≈0.75
0.7	≈0.50	1.4	≈0.5
0.8	≈0.70	1.6	≈0.3
0.9	≈0.85	1.8	≈0.15
1.0	1	2.0	0

Sine Function Generators

Similar functions can be formulated to approximate a SINE function converter as shown in Figure 22. With a linearly changing (0 to 5V) input the output will follow 0^o to 90^o of a sine function (0 to 5V) output. This configuration is theoretically capable of ±2.1% maximum error to full scale.

By adding a second HA-2556 to the circuit an improved fit may be achieved with a theoretical maximum error of 0.5% as shown in Figure 23. Figure 23 has the added benefit that it will work for positive and negative input signals. This makes a convenient triangle (±5V input) to sine wave (±5V output) converter.



$$V_{OUT} = V_{IN}\frac{(1 - 0.1284V_{IN})}{(0.6082 - 0.05V_{IN})} \approx 5\sin\left(\frac{\pi}{2}\cdot\frac{V_{IN}}{5}\right)$$

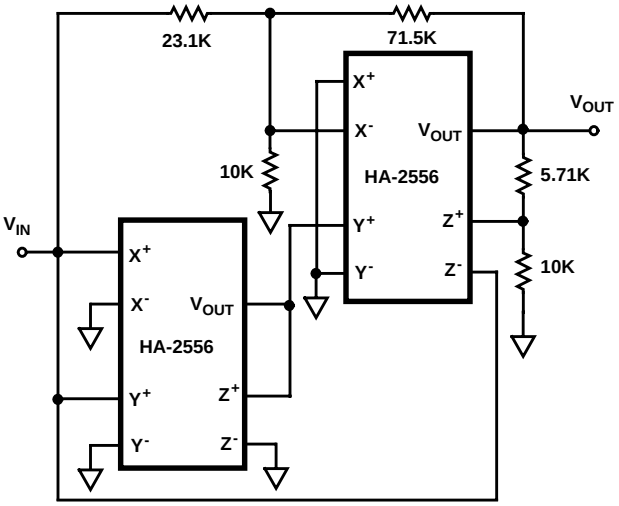
for; $0V \le VIN \le 5V$ max theoretical error = 2.1%FS

where:

$$0.6082 = \frac{R4}{R3 + R4}\ ; \qquad 5(0.1284) = \frac{R2}{R1 + R2}$$

$$5(0.05) = \frac{R6}{R5 + R6}$$

FIGURE 22. SINE-FUNCTION GENERATOR



$$V_{OUT} = \frac{5V_{IN} - 0.05494V_{IN}^3}{3.18167 + 0.0177919V_{IN}^2} \approx 5\sin\left(\frac{\pi}{2}\cdot\frac{V_{IN}}{5}\right)$$

$-5V \le V_{IN} \le 5V$ max theoretical error = 0.5%FS

FIGURE 23. BIPOLAR SINE-FUNCTION GENERATOR

Further Reading

1. Pacifico Cofrancesco, “RF Mixers and ModulatorsMade with a Monolithic Four-Quadrant Multiplier” Microwave Journal, December 1991 pg. 58 - 70.
2. Richard Goller, “IC Generates Nonintegral Roots” Electronic Design, December 3, 1992.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Intersil Semiconductor and is for use as application and design information only. No guarantee is implied.

TYPICAL PERFORMANCE CHARACTERISTICS

Device Tested at Supply Voltage = ±15V, R_F = 50Ω, R_L = 1kΩ, C_L = 20pF, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	TEMP	TYP	UNITS
Multiplication Error	ME	V_Y, V_X = ±5V	+25°C	±1.5	%FS
			+125°C, -55°C	±3.0	%FS
Multiplication Error Drift		V_Y, V_X = ±5V	+125°C, -55°C	±0.003	%FS/°C
Linearity Error	LE3V	V_Y, V_X = ±3V	+25°C	±0.02	%FS
	LE4V	V_Y, V_X = ±4V	+25°C	±0.05	%FS
	LE5V	V_Y, V_X = ±5V	+25°C	±0.2	%FS
Differential Gain	DG	f = 4.43MHz, V_Y = 300mV$_{P-P}$, V_X = 5V	+25°C	0.1	%
Differential Phase	DP	f = 4.43MHz, V_Y = 300mV$_{P-P}$, V_X = 5V	+25°C	0.1	Deg.
Scale Factor	SF		+25°C	5	V
Voltage Noise	E_N (1kHz)	f = 1kHz, V_X = 0V, V_Y = 0V	+25°C	150	nV/$\sqrt{Hz}$
	E_N (100kHz)	f = 100kHz, V_X = 0V, V_Y = 0V	+25°C	40	nV/$\sqrt{Hz}$
Positive Power Supply Rejection Ratio	+PSRR	V_S+ = +12V to +15V, V_S- = -15V	+25°C	80	dB
			+125°C, -55°C	80	dB
Negative Power Supply Rejection Ratio	-PSRR	V_S- = -12V to -15V, V_S+ = +15V	+25°C	55	dB
			+125°C, -55°C	55	dB
Supply Current	I_{CC}	V_X, V_Y = 0V	+25°C	18	mA
			+125°C, -55°C	18	mA
INPUT CHARACTERISTICS					
Input Offset Voltage	V_{IO}	V_Y = ±5V	+25°C	±3	mV
			+125°C, -55°C	±8	mV
Input Offset Voltage Drift	V_{IO}TC	V_Y = ±5V	+125°C, -55°C	±45	µV/°C
Input Bias Current	I_B	V_X = 0V, V_Y = 5V	+25°C	±8	µA
			+125°C, -55°C	±12	µA
Input Offset Current	I_{IO}	V_X = 0V, V_Y = 5V	+25°C	±0.5	µA
			+125°C, -55°C	±1.0	µA
Differential Input Range			+25°C	±5	V
Common Mode Range (V_X)	CMR (V_X)		+25°C	±10	V
Common Mode Range (V_Y)	CMR (V_Y)		+25°C	+9, -10	V
Common Mode (V_X) Rejection Ratio	CMRR (V_X)	V_XCM = ±10V, V_Y = 5V	+25°C	78	dB
			+125°C, -55°C	78	dB
Common Mode (V_Y) Rejection Ratio	CMRR (V_Y)	V_YCM = +9V, -10V, V_X = 5V	+25°C	78	dB
			+125°C, -55°C	78	dB
Common Mode (V_Z) Rejection Ratio	CMRR (V_Z)	V_ZCM = ±10V, V_X = 0V, V_Y = 0V	+25°C	78	dB
			+125°C, -55°C	78	dB
V_Y, V_Z CHARACTERISTICS (Note 1)					
Bandwidth	BW (V_Y)	-3dB, V_X = 5V, V_Y ≤ 200mV$_{P-P}$	+25°C	57	MHz
Gain Flatness	GF (V_Y)	0.1dB, V_X = 5V, V_Y ≤ 200mV$_{P-P}$	+25°C	5.0	MHz
AC Feedthrough	V_{ISO} (1MHz)	f_O = 1MHz, V_Y = 200mV$_{P-P}$, V_X = nulled (Note 2)	+25°C	-65	dB
	V_{ISO} (5MHz)	f_O = 5MHz, V_Y = 200mV$_{P-P}$, V_X = nulled (Note 2)	+25°C	-50	dB
Rise and Fall Time	T_R, T_F	V_Y = 200mV step, V_X = 5V, 10% to 90% pts	+25°C	8	ns
			+125°C, -55°C	8	ns

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Intersil Semiconductor and is for use as application and design information only. No guarantee is implied.

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at Supply Voltage = ±15V, R_F = 50Ω, R_L = 1kΩ, C_L = 20pF, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	TEMP	TYP	UNITS
Overshoot	+OS, -OS	V_Y = 200mV step, V_X = 5V	+25°C	17	%
			+125°C, -55°C	17	%
Slew Rate	+SR, -SR	V_Y = 10V step, V_X = 5V	+25°C	450	V/µs
			+125°C, -55°C	450	V/µs
Differential Input Resistance	R_{IN} (V_Y)	V_Y = ±5V, V_X = 0V	+25°C	1	MΩ
V_X CHARACTERISTICS					
Bandwidth	BW (V_X)	-3dB, V_Y = 5V, $V_X \leq 200mV_{P-P}$	+25°C	52	MHz
Gain Flatness	GF (V_X)	0.1dB, V_Y = 5V, $V_X \leq 200mV_{P-P}$	+25°C	4.0	MHz
AC Feedthrough	V_{ISO} (1MHz)	f_O = 1MHz, $V_X = 200mV_{P-P}$, V_Y = nulled (Note 2)	+25°C	-65	dB
	V_{ISO} (5MHz)	f_O = 5MHz, $V_X = 200mV_{P-P}$, V_Y = nulled (Note 2)	+25°C	-50	dB
Rise & Fall Time	T_R, T_F	V_X = 200mV step, V_Y = 5V, 10% to 90% pts	+25°C	8	ns
			+125°C, -55°C	8	ns
Overshoot	+OS, -OS	V_X = 200mV step, V_Y = 5V	+25°C	17	%
			+125°C, -55°C	17	%
Slew Rate	+SR, -SR	V_X = 10V step, V_Y = 5V	+25°C	450	V/µs
			+125°C, -55°C	450	V/µs
Differential Input Resistance	R_{IN} (V_X)	V_X = ±5V, V_Y = 0V	+25°C	1	MΩ
OUTPUT CHARACTERISTICS					
Output Resistance	R_{OUT}	V_Y = ±5V, V_X = 5V, R_L = 1kΩ to 250Ω	+25°C	0.7	Ω
Output Current	I_{OUT}	V_{OUT} = 5V, R_L = 250Ω	+25°C	±45	mA
			+125°C, -55°C	±45	mA
Output Voltage Swing	$+V_{OUT}$	R_L = 250Ω	+25°C	±6.05	V
			+125°C, -55°C	±6.05	V

NOTES:

1. V_Z AC characteristics may be implied from V_Y due to the use of V_Z as feedback in the test circuit.
2. Offset voltage applied to minimize feedthrough signal.